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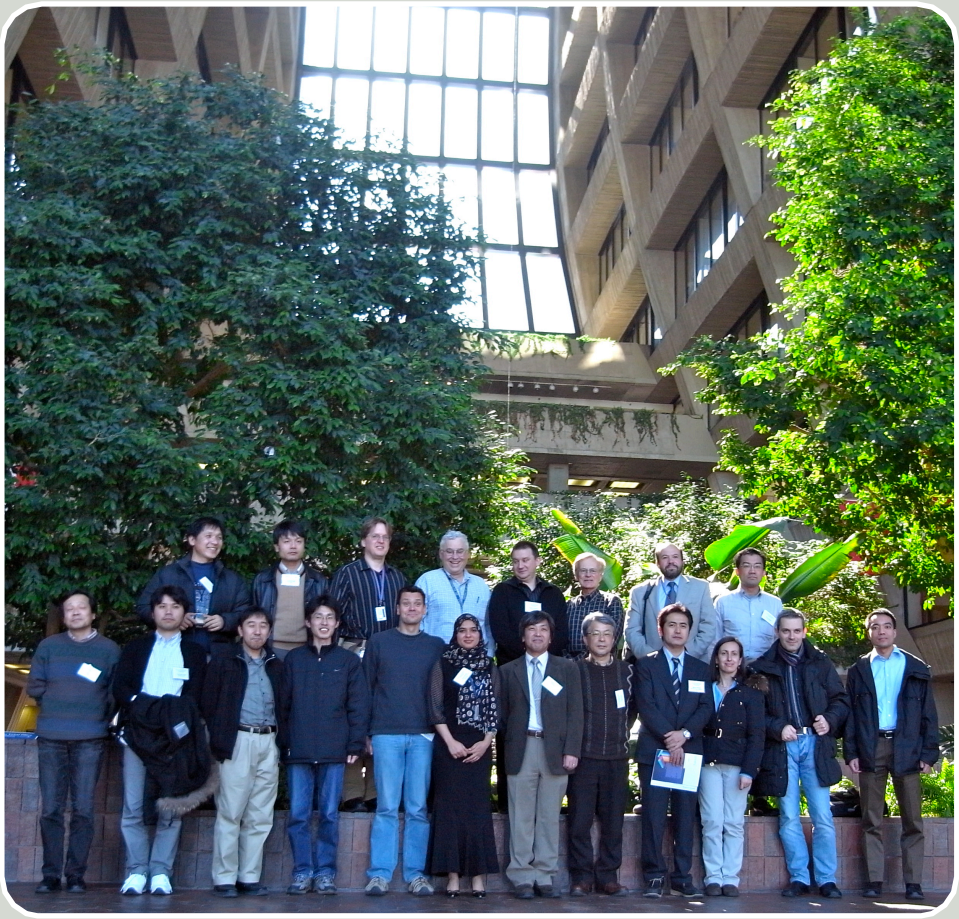
FEATURE STORY



Thriving new detector technology: SOIPIX

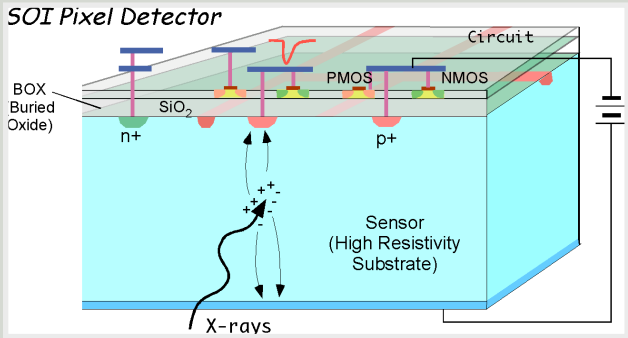
[Silicon-on-insulator, Pixel Detector]

On March 4-5, 2010, KEK's detector scientists and international collaborators from around the world gathered in a meeting room at Fermilab to discuss a new detector technology: silicon-on-insulator pixel (SOIPIX). Learn about KEK's new technological endeavor, and the recent steps made by collaborators to make this powerful new technology work.

Participants of the 5th SOI collaboration meeting gather in the Wilson Tower at Fermilab for a group photo.

For detector scientists, this new technology may be revolutionary, changing the way some types of the particle and photon sensors are fabricated (or built). The technology is called silicon-on-insulator pixel or SOIPIX. This innovative technology is starting to draw attention from the world detector technology community for its high speed, high spatial resolution, low power consumption, and compactness.

In general, detecting particles or photons requires two devices: a sensor, and it's associated readout electronics. For a silicon sensor, detector scientists conventionally use services of semiconductor companies specialized in processing of devices on high resistivity substrates. For the electronics to be connected to the detector, integrated circuit technology called complementary metal-oxide semiconductor (CMOS) is commonly used. Interactions of particles or photons in silicon sensor produce secondary electrons and electron holes. These secondary electrons and holes are converted into a voltage pulse, which is then amplified to produce a usable signal. When constructed with conventional CMOS technology, these two components (readout electronics and sensor) are produced separately, and then mechanically bonded by a technique called bump-bonding. In SOI, the two parts are produced together on a single chip. Only an insulating layer of sub-micron in thickness separates the readout electronics part and its silicon substrate. The ingenuity of the detector scientists is that they use the silicon substrate as the sensor.



Silicon-on-insulator pixel (SOIPIX) is a technology that combines the sensor and readout electronics on a single semiconductor device.

The SOI technology isn't new. It has been around for three decades. Because the electrical separation of electronics and the substrate reduces the parasitic capacitance in the device, it speeds up the readout. The insulator also reduces the leakage current,

From right: Prof. Yasuo Arai of KEK, the leader of the SOI group; Mr. Ikuo Kurachi from OKI Semiconductor Co. Ltd.; Jun Uchida, a graduate student from Osaka University; and Dr. Yoshiyuki Onuki, a postdoc at Tohoku University.

lowering the power consumption of the device. Thus, SOI devices are faster and consume less power than conventional CMOS technology. SOI technology is already used in some CPUs, game devices, digital watches, and in aerospace engineering. Unfortunately, the higher cost of producing SOI chips has prevented it from becoming widely used.

For the detector, SOI provides many more advantages. First, because of the very thin substrate (~40 nm) of the electronics part, the electronics are affected less by charges produced by radiation in the substrate. The radiation hardness is particularly important for use in particle accelerator and in space. Second, SOI transistors can tolerate a broad range of temperatures compared to standard CMOS technology. This makes them convenient for use in extreme conditions such as in space. Third, because of the insulator between pixels, each pixel is electrically less affected by the neighboring pixels. This means that pixel size can be reduced, improving spatial resolution dramatically. Finally, the thickness of the sensor can be adjusted. This means that the sensor can be made as thick or thin as desired, as long as the appropriate amount of voltage can be applied to it for particle detection. Pixel detectors using SOI technology can provide an ideal detector for high energy particles, and photons X-rays up to a dozen or so keV.

Open SOIPIX collaboration

The idea of using SOI technology for a particle detector is also not new. It has been around for a decade. European scientists started investigating the technology some time ago, but they soon abandoned the idea because the semiconductor technology they were using did not give the desired results. Later, in 2005, the idea was picked up by Prof. Yasuo Arai at KEK, the leader of the SOI group in the KEK Detector Technology Project (DTP). He saw vibrant opportunity in the technology, an opportunity to bring cutting-edge technology to the world, technology from Japan.

"As I researched the SOI technology, I found out that Japan had a very strong technological background in SOI," says Arai. "The detector had enormous potential that was not fully explored, and yet the problems were tractable using the advanced semiconductor processing technology we had in our country."

Arai's strategy was to make the SOIPIX processes they developed open to everyone. "Openness invites competition, and brings about rapid advancement in SOIPIX technology," says Arai. He called for collaborations overseas, and now the SOIPIX group is the best funded and largest international group among the eight DTP projects at KEK. In 2006, the team was joined by several US laboratories, including Fermilab, Lawrence Berkeley National Laboratory (LBNL), and University of Hawaii. More recently, they have also been joined by several institutions from Europe.

SOIPIX collaboration meets at Fermilab

The SOIPIX collaboration now has around 100 member scientists from 16 institutions. The 5th collaboration meeting was held at Fermilab on 4-5 March of this year, and was the first formal SOI meeting held outside Japan. Around 30 participants from 10 research institutions attended. Participants came from Belgium, Italy, Japan, Poland, and US, and from two Japanese companies: OKI Semiconductor Co. Ltd. (OKI Semiconductor) and ZyCube Co. Ltd. (ZyCube). While most attendees were present on-site, some attended via remote link. All enjoyed intense discussions on their new results.

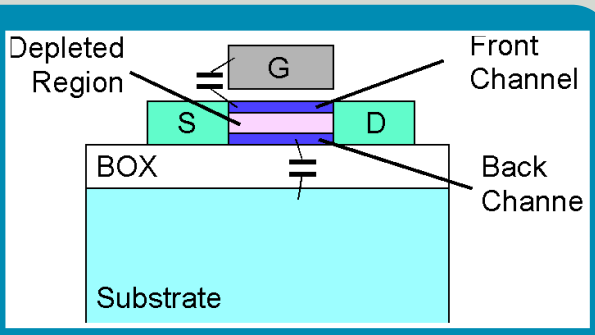
The SOIPIX collaboration is formed by physicists and engineers who wish to use the technology in their future projects in high energy particle sciences. Important possible applications include the Belle II detector in KEK's B Factory experiment, the upgrade of the LHC's ATLAS detector and future Linear Collider experiments. Because of its high spatial resolution, SOI is an ideal solution for the vertex detectors that measure particle tracks very close to the interaction point. "However, applications of SOI detector technology can be extended beyond particle science, in medical imaging, astrophysics, and electron microscopy," says Arai.

Making it work—a challenge of back-gate problem

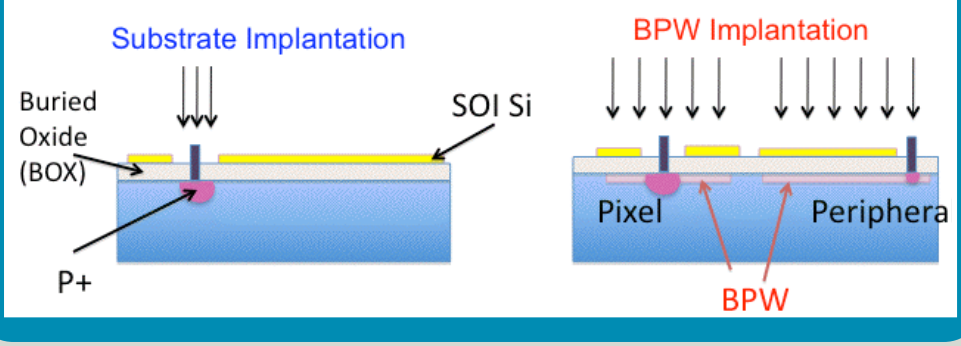
SOI has a layer of buried silicon oxide as an insulator between the electronics and the substrate. For commercial use, this is all that is needed for an SOI device, because the only component of interest is the electronics.

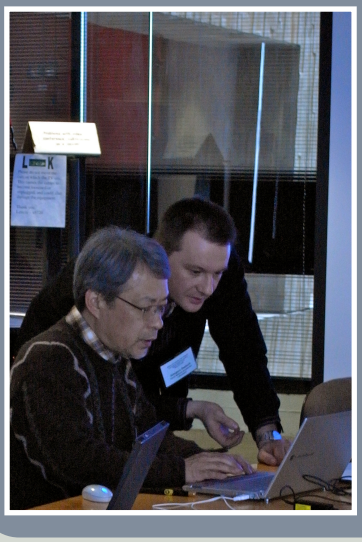
For detectors, however, the silicon substrate acts as a sensor, and the signals from the sensor need to be read out by the electronics. In order to give the readout electronics access to the sensor, holes are etched through the buried oxide insulator and filed with conductive material, typically tungsten, to form conductive contacts, and p-type and n-type silicon islands —silicon that can conduct electricity—are formed beneath the oxide layer. The junction of two types of silicon allows one-way flow of

→The back gate problem occurs when a voltage is applied to the substrate in order to detect radiation.



↓Buried p-wells (BPW) have proven to be a successful solution to the back gate problem. Boron ions are implanted around the p-type silicon in this image.





Dr. Grzegorz Deptuch (right) of Fermilab discusses with Prof. Yasuo Arai of KEK, the leader of the SOI group (left).

current. The detection of a particle is seen as freeing some excess charge in the detector bulk. The electric field present due to the existing junction causes drifting of charge carriers to an implantation island, which are read out via a tungsten plug through the hole to the electronics. Each pixel must have at least one through-buried-oxide-hole representing the pixel. The distance between holes can be as small as 1 micrometer, which allows for high spatial resolution.

"At first, we thought that simply inserting an oxide insulator between silicon layers would produce an SOI detector. But when we looked more closely, we found out that it would not work because the sensor and electronics have strong coupling," explains Arai. To detect radiation, a voltage needs to be applied to the sensor side of the device. This creates a depletion region in the silicon, an area where no charge carriers are present. The back-end of the transistor is capacitively connected to the substrate, and at the same time grounded by the source voltage at the front-end. This means that a voltage difference can develop between the front and back of the transistor, when a voltage is applied to the substrate. This is called the back-gate effect.

The problem with the back-gate effect is that the voltage rise can cause the transistor to turn on, which would cause the pixel to no longer work. The effect imposes an upper limit of 10 to 15 volts on the back of the substrate, which in turn limits the thickness of the depletion region.

In discussion with OKI Semiconductor engineers, Arai and his team came up with a solution to the back-gate problem. The solution was to add buried p-wells (BPWs) to the detector. Arai and his team implanted boron ions into the silicon around the pixel right beneath the buried oxide. The tungsten plug can then be used to control the voltage of the boron well, and therefore the voltage beneath the transistors. This solves the back-gate problem.

"At first, there were many uncertainties as to the influence of implantation on the transistor above and uncertainty as to how thick the well needs to be," says Arai. The team simulated and calculated the effects and found that just a shallow well could make a great deal of difference. They developed a process to create the buried p-wells, and built a prototype to test the solution.

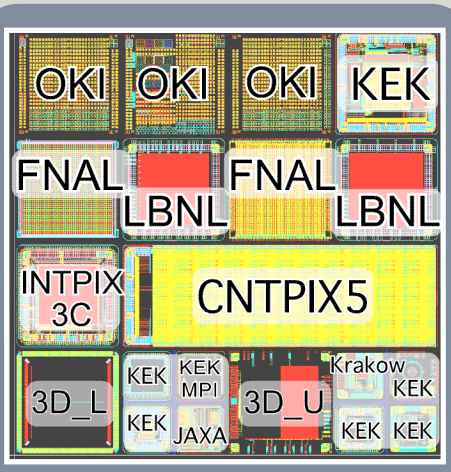
The result of the BPW test was remarkable. This modification raised the maximum substrate bias voltage to above 130 volts. The team further found that using the boron implantation method also reduces the pixel size and improves radiation hardness. The functioning of an SOI detector with BPW technology was proven in Japan a year ago, and has since been investigated for SOI detectors by other groups worldwide.

At the recent SOIPIX collaboration meeting, groups from Institute of Nuclear Physics at Krakow (Poland), Lawrence Berkeley National Laboratory (LBNL), and Fermilab all reported separate results showing that the BPW solution gave successful results.

"We can now say that the issue of the back-gate has been resolved. Now we need to tackle the next issue," says Arai. Currently, some operation of the readout electronics causes crosstalk in the sensor. To amend this, a new nested double well structure is being discussed at Fermilab, KEK, and OKI Semiconductor. An organizer of the collaboration meeting, Dr. Grzegorz Deptuch of Fermilab, gave a presentation on benefits of the simultaneous use of buried n-wells (BNW) and buried p-wells (BPW) in a form of one well containing another. The scheme is called nested wells. The technology and possible future development in the issue were discussed. "The availability of buried nested wells on the next multi-project wafer run is great news," Deptuch pointed out during his talk.

OKI semiconductor's presence in SOI

OKI Electric Industry Co., Ltd. was the only company in the world that mass-produces fully-depleted type SOI chips. When Arai started out with his project, there was an important prerequisite to gain OKI's cooperation for the idea of an SOI detector.

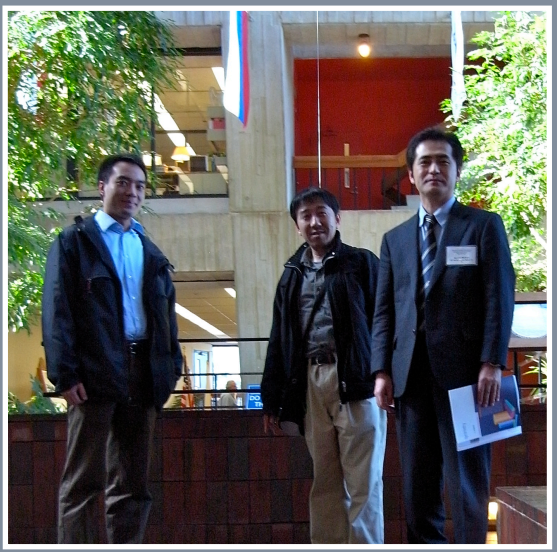


The production of advanced semiconductor chips is an expensive business. Each Multi Project Wafer (MPW) run accommodates multiple designs submitted by the member institutions that conduct SOIPIX R&D.

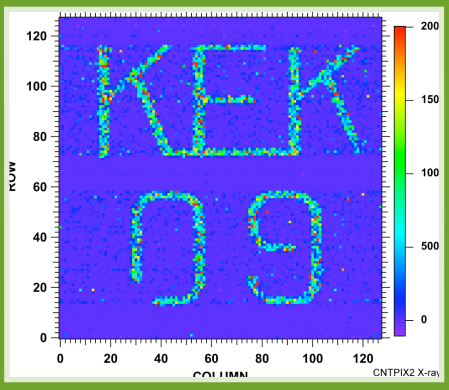
"Without industry cooperation, our project cannot exist," says Arai. For OKI as well, SOI's high price range demanded applications beyond mass use. A detector for high energy physics may be just such application.

The two parties found they had common interests. The partnership continued even after OKI's electronics division was taken over by Rohm Co. Ltd. in 2008 to form OKI Semiconductor Co., Ltd. In fact, the partnership grew even stronger. "It took some convincing," recalls Arai. He and his colleagues from overseas visited the company and successfully argued that pursuit of academic interests has significance, and that there is great potential in SOI beyond Japan and beyond high energy physics.

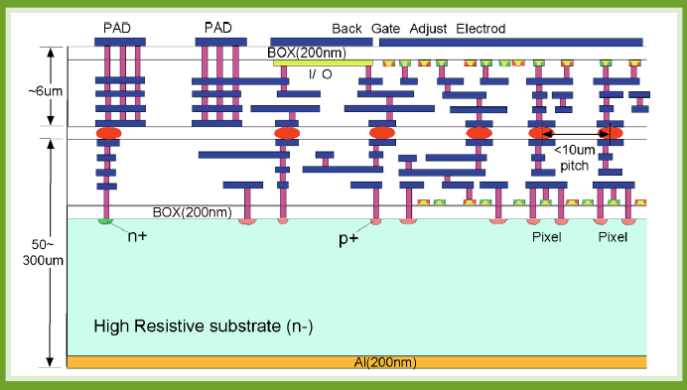
Two of OKI Semiconductor's professional engineers were also present at the collaboration meeting, and explained the current status of the project. "We often meet with KEK people, but in this meeting we were able to meet and hear from people from other



(From left) Lawrence Soung Yee, a PhD student from the Univ. Cathlique de Lauvain in Belgium; Dr. Toshinobu Miyoshi from KEK, and Mr. Masao Okihara from OKI Semiconductor Miyagi Co. Ltd.



An X-ray image detected by SOI last year.



Micro-bump technology developed by ZyCube Co. Ltd. will be investigated using OKI Semiconductor's SOI process for vertical integration.

oversea institutions like Fermilab and LBNL," says Mr. Masao Okihara of OKI Semiconductor. "Characteristics such as radiation hardness, hysteresis effect, and noise parameters are something we are not very well acquainted with in the course of conventional SOI development, but they are important for the SOIPIX detector collaboration."

The demand for OKI Semiconductor's SOI processes is high, and is gathering great interest from new SOIPIX collaboration members as well. Lawrence Soung Yee, a PhD student from the Université Catholique de Louvain in Belgium, has been investigating the SOI process using the university's in-house technology. He says: "For the next generation we are thinking OKI Semiconductor technology. It is more advanced technology than what we have right now."

SOIPIX's new direction—vertical integration

An exciting recent development in SOIPIX is the 3D integration of circuits. "Vertical integration can remove some of the problems that are associated with SOIPIX processes, by decoupling the sensor and readout processes," says the head of the ASIC Development Group at Fermilab, Dr. Raymond Yarema. "The 3D technology uses new ideas about how to create connections between sensors and readout electronics. This allows lower mass components and lower cost connections between the sensor and the readout electronics."

The leader of the KEK Detector Technology Project (DTP). Prof. Junji Haba talks with the head of the ASIC Development Group at Fermilab, Dr. Raymond Yarema about vertical integration during a coffee break at the recent SOIPIX collaboration meeting.

During the meeting, a Japanese venture company, ZyCube, presented one such technology called micro-bump technology which was developed by Tohoku University. ZyCube promotes this technology and has been working with OKI Semiconductor. "If this becomes a successful development, it will find use beyond the SOI process. It could be used for CMOS and other technologies for doing 3D or vertical integration. In that sense, detector SOI technology could produce important spin-offs."

Efforts in vertical integration are facilitated by institutions from Europe, the US, and Japan. KEK and Fermilab play central roles. "A consortium of parties interested in vertical integration was initiated by Fermilab and now involves 16 institutions. This is about the same size as the SOIPIX collaboration. We pursue somewhat different approaches and applications," says Yarema. The consortium is exploring applications for such experiments as the LHC, the B Factory in Italy, and new light sources.

One big step forward

When Arai started advertizing the project oversea, US institutions were the first to join the collaboration. Since then, many institutions from countries in Europe and Asia, as well as from other disciplines such as astronomical observatories within Japan, have expressed interest.

"The meeting at Fermilab was a great opportunity for us to bring in interested oversea parties," says Arai. "Japanese projects tend to be self-contained, and a lot of times, materials are not available in English. Many questions were asked and answered during the meeting, and the collaboration as a whole has just seen a big step forward in terms of the technology as well."

In his concluding remarks, Yarema said: "The analysis leading to the nested buried well concept, and ideas beyond this, show that there is much to explore in future runs, and that this should lead to many interesting talks at future meetings."

The head of KEK DTP, Prof. Junji Haba, was also present. "KEK has a strong interest in pursuing the SOI detector technology. The flank discussions held at the meeting between industry and oversea project groups will certainly motivate the advancement of the technology." Arai's goal: to increase the proportion of SOI designs submitted by oversea institutes. Right now, KEK takes up about a half. The next set of submissions will be this summer.

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